

**WHAT IS CLAIMED IS:**

1. A device for selecting a normal circuit in a communication system comprising:

at least one pair of general function circuit modules;

one pair of control function circuit modules, each of the control function circuit modules including at least one first selecting circuit that selects one of the two general function circuit modules in each of said at least one pair that is in normal operation and provides a respective function failure signal when the control function circuit modules have function failure;

one pair of power supply modules that supply power to the modules and provide a respective power fail signal when a power failure occurs;

a separate processor that controls the modules; and

a second selecting circuit that switches states of the two control function circuit modules responsive to the control of the processor and the failure signals, wherein the second selecting circuit switches the control function circuit module of the pair in an active state to a standby state after switching the control function circuit module of the pair in the standby state to the active state.

2. The device as claimed in claim 1, wherein the processor enables read/write states of the control function circuit module in the active state, and wherein the processor enables only a read state of the control function circuit module in the standby state to prevent an output state of the control function circuit module in the active state from being changed by the output state of the control function circuit module in the standby state.

3. The device as claimed in claim 1, wherein when the second selecting circuit switches states of the control function circuit module in the standby state and the control function circuit module in the active state to the other, the control function circuit module in the active state first informs the control function circuit module in the standby state of the switching by the second selecting circuit for preventing output states of the control function circuit module in the standby state and the control function circuit module in the active state from being enabled at the same time.

4. The device as claimed in claim 1, wherein the second selecting circuit comprises:

a first selecting part that provides an output enable signal to the first control function circuit module in response to state signals from the processor, the power fail signal from the first power supply module among the two power supply modules, and the function failure signal from the first control function circuit module among the two control function circuit modules; and

a second selecting part that provides an output enable signal to the second control function circuit module in response to the state signals from the processor, the power fail signal from the second power supply module among the two power supply modules, and the function failure signal from the second control function circuit module among the two control function circuit modules, wherein the first selecting part and the second selecting part exchange their corresponding state information so that one of the first control function circuit module and the second function circuit module that is in normal operation is selected to be in the active state.

5. The device as claimed in claim 4, wherein the first selecting part comprises:  
a first reset switch;

a first processor interfacing part for receiving the state signals from the processor;

5 a first OR gate for logically processing an output signal of the first reset switch and an initial state signal of the first processor interfacing part;

a first inverter for inverting the power fail signal from the first power supply module;

10 a second OR gate for logically processing an output signal of the first inverter and the function failure signal of the first control function circuit module;

a second inverter for inverting an output signal of the second OR gate;

a first AND gate for logically processing a first state signal from the second selecting part and an output signal of the first OR gate;

15 a third inverter for inverting a second state signal from the second selecting part;

a first D flipflop having a clear terminal for receiving an output signal of the third inverter, an input terminal for receiving an output signal of the first AND gate, a set terminal for receiving an output signal of the second inverter, and an output terminal for providing an output signal that selectively enables the first control function circuit module responsive to the received signals;

20 a third OR gate for logically processing an output signal of the first OR gate and an output signal of the second OR gate and outputting a first state signal to the second selecting part;

25 a fourth inverter for inverting the output signal of the first D flipflop and outputting a selection signal for reading an output state of the second control function circuit module and a second state signal to the second selecting part;

a first exclusive OR gate for logically processing the initial state value of the first processor interfacing part and the output signal of the first D flipflop and outputting a first interrupt signal to the processor; and

30 a first clock providing part for providing a first clock signal to the first D flipflop, wherein the processor makes the output signal of the first D flipflop and the initial state value of the first processor interfacing part equal, and the first clock providing part provides the first clock signal having a cycle period the same with a second clock signal of the second selecting part or the second clock signal inverted to the first selecting part, and wherein the cycle period of the first clock signal is different from a cycle period of a system clock by a prescribed cycle period is provided to the first D flipflop when the state of the first control function circuit module is switched.

6. The device as claimed in claim 5, wherein the first clock providing part comprises:

a delay for multiplying the system clock signal by a quarter cycle period;  
a second exclusive OR gate for logically processing an output signal of the delay and the system clock; and

5 a third exclusive OR gate for logically processing a logic signal dependent on a location of insertion of the first control function module and an output signal of the second exclusive OR gate.

7. The device as claimed in claim 5, wherein the state signals provided from the processor to the first processor interfacing part includes a read enable signal, a write enable signal, a data, and an address.

8. The device as claimed in claim 5, wherein the first D flipflop is a positive edge triggered flipflop.

9. The device as claimed in claim 4, wherein the second selecting part comprises:

a second reset switch;

a second processor interfacing part for receiving the state signals from the processor;

a fourth OR gate for logically processing an output signal of the second reset switch and an initial state signal of the second processor interfacing part;

a sixth inverter for inverting the power fail signal from the second power supply module;

a fifth OR gate for logically processing an output signal of the sixth inverter and the function failure signal of the second control function circuit module;

a seventh inverter for inverting an output signal of the fifth OR gate;

a second AND gate for logically processing a second state signal from the first selecting part and an output signal of the fourth OR gate;

an eighth inverter for inverting a first state signal from the first selecting part;

a second D flipflop having a clear terminal for receiving an output signal of the eighth inverter, an input terminal for receiving an output signal of the second AND gate, a set terminal for receiving an output signal of the seventh inverter, and an output terminal for providing an output signal that selectively enables the second control function circuit module responsive to the received signals;

a sixth OR gate for logically processing an output signal of the fourth OR gate and an output signal of the fifth OR gate and outputting a second state signal to the first selecting part;

25 a ninth inverter for inverting the output signal of the second D flipflop and outputting a selection signal for reading an output state of the first control function circuit module and a first state signal to the first selecting part;

a fourth exclusive OR gate for logically processing the initial state value of the second processor interfacing part and the output signal on the second D flipflop and  
30 outputting a second interrupt signal to the processor; and

a second clock providing part for providing a second clock signal to the second D flipflop, wherein the processor makes the output signal of the second D flipflop and the initial state value of the second processor interfacing part equal in response to the second interrupt signal, and the second clock providing part provides the second clock having a cycle period equal to a first clock signal of the first selecting part or the first clock signal inverted to the second selecting part, or the second clock providing part provides the second clock signal having the cycle period different from a cycle period of a system clock by a prescribed cycle period to the second D flipflop when the state of the second control function circuit module is converted.

10. The device as claimed in claim 9, wherein the second clock providing part comprises:

a delay for multiplying the system clock signal by a quarter cycle period;

a fifth exclusive OR gate for logically processing an output signal of the

5 delay and the system clock; and

a sixth exclusive OR gate for logically processing a logic signal dependent on a location of insertion of the second control function module and an output signal of the fifth exclusive OR gate.

11. The device as claimed in claim 9, wherein the state signals provided from the processor to the second processor interfacing part includes a read enable signal, a write enable signal, a data, and an address.

12. The device as claimed in claim 9, wherein the first D flipflop is a positive edge triggered flipflop.

13. The device as claimed in claim 1, wherein the first selecting circuit comprises:

a first state input part that collects state information of the pairs of the first general function circuit modules and provides at least one alarm signal, and also provides a selection state of the first general function circuit module of the opposite control function circuit module;

a second state input part that collects state information of the pairs of the second general function circuit modules and provides at least one alarm signal, and also provides a selection state of the second general function circuit module of the opposite control function circuit module;

a processor state input part that provides selection information, and write enable, shift clock, and port enable signals on the general function circuit modules of the opposite control function circuit module;

a first NOR gate for logically processing the alarm signals from the first state input part;

a first buffer for buffering the selection state of the first general function circuit module from the opposite control function module according to a read selection state of a relevant control function circuit module;

a first AND gate for logically processing output signals of the first NOR gate and the first buffer;

a first D flipflop having an input terminal D for receiving the write enable signal from the processor state input part, a clock terminal for receiving the shift clock signal, a clear terminal for receiving the port enable signal, and an output terminal for providing an output signal;

a first NOR gate for logically processing the alarm signals from the second state input part;

a second buffer for buffering the selection state of the second general function circuit module from the opposite control function module according to the read selection state of the relevant control function circuit module;

a second AND gate for logically processing output signals of the first NOR gate and the second buffer;

a second D flipflop having an input terminal for receiving selection information on the general function circuit module of the opposite control function circuit module from the processor state input part, a clock terminal for receiving an output signal of the first D flipflop, a set terminal for receiving an output of the first AND gate, a clear terminal for receiving an output of the second AND gate, and output terminals for providing an output signal and an inverted output signal;

a third D flipflop having an input terminal for receiving selection information on the general function circuit module of the opposite control function circuit module from the processor state input part, a clock terminal for receiving an output signal of the first D flipflop, and a terminal for providing an output signal;

a third buffer for buffering the output signal and the inverted output signal of the second D flipflop depending on the output selection state of the relevant control function circuit module and outputting a selection signal that selects the general function circuit module that operates normally among said each pair of the general function circuit modules; and

an exclusive OR gate for logically processing output signals of the second D flipflop and the third D flipflop and outputs to the processor a third interrupt signal, wherein the processor maintains states of the output terminal on the second D flipflop and the input terminal the same in response to the third interrupt signal.

14. A device as claimed in claim 13, wherein the first, second and third D flipflops are positive edge triggered flipflops.

15. A device as claimed in claim 13, wherein the alarm signals of the first state input part and the second state input part include one of function alarm signals, reset alarm signals, common power fail alarms and open alarm signals of general function circuit modules.

16. A device for selecting a normal circuit in a communication system comprising:

a plurality of pairs of circuit module means;

first and second control circuit module means, wherein the first and second control circuit module means include a first selecting means that selects one of the two circuit module means in a selected pair and provides a respective function failure signal when the control circuit module means have a function failure;

a separate control means that controls the device for selecting a normal circuit; and

10 a second selecting means that switches states of the two control circuit module means according to the control of the control means and the failure signals, for switching the first control circuit module means in an active state to a standby state after switching the second control circuit module means in the standby state to the active state.

17. The device as claimed in claim 16, further comprising one pair of power supply module means that supply power to the module means and provide a power fail signal when a power failure occurs.